



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/001,478	11/01/2001	Craig Nemecek	CYPR-CD01213M	6435

7590 04/02/2007
WAGNER, MURABITO & HAO LLP
Third Floor
Two North Market Street
San Jose, CA 95113

EXAMINER

PROCTOR, JASON SCOTT

ART UNIT	PAPER NUMBER
----------	--------------

2123

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/02/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.		Applicant(s)	
	10/001,478		NEMECEK ET AL.	
	Examiner		Art Unit	
	Jason Proctor		2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 February 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2,4-10,12 and 14-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2,4-10,12 and 14-23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 January 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claims 1-2, 4-10, 12, and 14-21 were rejected in the office action of 5 September 2006.

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6 February 2007 has been entered.

Applicant's submission filed on 6 February 2007 has amended claims 1, 4, 5, 7, 8, 10, 12, 15, 16, 18, and 19; and presented new claims 22 and 23. Claims 1-2, 4-10, 12, and 14-23 are pending in this application.

Claims 1-2, 4-10, 12, and 14-23 are rejected.

Priority

1. This Application contains a claim for the benefit of priority to U.S. Provisional Application No. 60/243,708 filed 26 October 2000. The provisional application has been reviewed and priority is denied, because the provisional application does not appear to enable the claimed invention as required under 35 U.S.C. Section 112, first paragraph. See 35 U.S.C. § 119(e)(1).

For example, the provisional application contains a set of 'powerpoint-style' drawings and datasheets describing desired features for a microcontroller or a 'system-on-chip,' but this material does not appear to contain either the text description or the drawings found in the

Art Unit: 2123

Application. In particular, no part of the provisional application appears to disclose the method steps shown in the Application at Fig. 7.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. § 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-2, 4-10, 12, and 14-23 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Independent claims 1, 10, and 12 recite the phrase “executing a set of boot code to *substantially* carry out initialization” which renders the claims vague and indefinite. It is unclear what constitutes “substantially” carrying out initialization. It is unclear if this means that some portion of the initialization is not performed by the boot code, or if the boot code also performs some function in addition to carrying out initialization. It is unclear what would be meant by a microcontroller that has been “substantially” initialized.

The term “substantially” in this context appears to be a relative term which is not defined by the claim. For example, it is unclear whether 50% initialized, 75% initialized, or 99% initialized would constitute “substantially” initialized. These values are merely exemplary.

Claims rejected but not specifically mentioned stand rejected by virtue of their dependence.

Response to Arguments – 35 USC § 102

Art Unit: 2123

3. In response to the previous rejection under 35 U.S.C. § 102 of claims 1, 10, and 12 as being anticipated by Coker, Applicants argue primarily that:

In contrast, Coker discloses that a shadow system executes the same software as the target-ECS from system start-up or reset (see Coker, col. 2, lines 56-58)... Claim 1 has been amended to further distinguish over Coker by reciting a limitation whereby at least one portion of the set of timing code is different from the set of boot code, as claimed.

The Examiner respectfully traverses this argument as follows.

Coker does disclose that the shadow system executes the same software as the target-ECS. Coker also discloses that at least one portion of the shadow system's operation is different from the target-ECS mode of operation (column 2, line 63 – column 3, line 12). In particular, Coker specifically discloses that the shadow system central processing unit performs “numerical operations” (i.e., executes software instructions) to send outputs to specific locations within its RAM rather than to complex output registers (in contrast to the target-ECS software). (*Id.*)

Therefore, although the amendments to the claim language are noted, this claim limitation does not distinguish over Coker because Coker expressly discloses that at least one portion of the timing code (shadow system software) is different from the boot code (target-ECS software).

This argument has been fully considered but has been found unpersuasive.

4. With regard to the limitation whereby at least one portion of the boot code is inaccessible to the virtual microcontroller, Applicants argue that:

Coker specifically teaches that the shadow system and the target-ECS function exactly the same by virtue of executing the same software. As such, Coker teaches that the same software is accessible to both the shadow system and the target-ECS and that they both execute the same software. Accordingly, Coker not only fails to teach that at least portion of the boot code is inaccessible to the virtual microcontroller, as claimed but it teaches away by teaching that the same software is executed by the shadow system and the target-ECS.

Art Unit: 2123

The Examiner respectfully traverses this argument as follows.

The text of the Coker reference plainly discloses that there are differences between the operation of the target-ECS and the shadow system, and therefore the software code executed by the target-ECS and the shadow system, as explained above.

Further, presuming *arguendo* that the target-ECS and the shadow system execute precisely the same code, this in no way suggests that the target-ECS code is accessible to the shadow system. For the target-ECS code to be accessible to the shadow system, the Coker reference would need to disclose or otherwise suggest that a mechanism actually exists in the Coker invention whereby the shadow system can read from, write to, or receive by transmission the target-ECS code. There is no such disclosure in the Coker reference.

This argument has been fully considered but has been found unpersuasive.

5. With regard to the limitation of simultaneously halting the microcontroller and the virtual microcontroller, Applicants argue that:

Coker discloses that the execution states of the shadow system will lag slightly behind that of the target-ECS because of the slight time delay but the time when any given instruction is executed will directly correspond to the execution state of the target-ECS when the same instruction was executed (see Coker, col. 8, lines 41-49). By definition, if the shadow system lags behind the target-ECS, then they cannot halt simultaneously, as claimed.

The Examiner respectfully traverses this argument as follows.

Applicants' argument is counter to the teachings of Applicants' specification, which explicitly states (page 20, lines 10-19):

By operating in the manner described, any breakpoints can be guaranteed to occur in a manner such that both the virtual microcontroller 200 and the microcontroller 232 halt operation in an identical state. Moreover, although the virtual microcontroller 220 and the microcontroller 232 operate on I/O data obtained at different times, both microcontroller are in complete synchronization by the time each SOI signal occurs. Thus, the virtual microcontroller 220 and the microcontroller 232 can be said to operate in lock-step with respect to a common time reference of the SOI signal as well as with respect to execution of

Art Unit: 2123

any particular instruction within a set of instructions being executed by both virtual microcontroller 220 and the microcontroller 232.

The claim limitations are interpreted in light of the specification (MPEP 2111). The prior art reference, as described by Applicants above, clearly anticipates any reasonable interpretation of the claim language in light of the specification.

This argument has been fully considered but has been found unpersuasive.

6. Applicants further argue that:

Moreover, the rejection asserts that it is inherent that a computer process in a debugger system halts because there is a distinct conclusion to the debugging process. The Applicants disagree because it is possible to log the information for debugging purposes and analyzing the logged information at a later time. Therefore, it is not inherent that a computer process in a debugger system halts as suggested by the rejection.

The Examiner responds to this argument as follows.

Applicants argument does not describe what is known in the art as a “breakpoint”. Applicants’ attention is respectfully drawn to page 16, Table 1.1, of “How Debuggers Work” by Jonathan B. Rosenberg. Table 1.1 states: “Breakpoints: halt execution at certain points to look for problems, such as incorrect variable types, mixups in variable names, flaws in logical comparisons, endless loops, garbled output, problems with arrays, and so on”. Applicants’ argument appears to describe what is known in the art as a “trace” instruction, and not a breakpoint.

However, the Coker reference discloses “a computer system and method for debugging, verifying, and developing an embedded computer system” but fails to describe several old and well-known debugging tools and techniques. Therefore, the previous rejection under 35 U.S.C. § 102 has been withdrawn.

Art Unit: 2123

7. Regarding claim 10, Applicants further argue that:

As discussed above, Coker fails to teach or suggest halting the microcontroller and the virtual microcontroller, as claimed. Accordingly, Coker also fails to teach or suggest removing the break, as claimed for similar rationale.

The Coker reference discloses “a computer system and method for debugging, verifying, and developing an embedded computer system” but fails to describe several old and well-known debugging tools and techniques. Therefore, the previous rejection under 35 U.S.C. § 102 has been withdrawn.

Response to Arguments – 35 USC § 103

8. The previous rejections based primarily upon the Tzori reference are withdrawn in response to the amendments to the claim language, particularly in response to the limitation that “at least one portion of said set of timing code is different from said set of boot code.” Applicants’ arguments have been fully considered but, in light of the new grounds of rejection, are moot.

Applicants submit that:

Applicants respectfully submit that taking Official Notice and inherency for almost half of the claims is contrary to judicious application. (Applicants’ remarks, 6 February 2007, page 20, emphasis in original)

In response, the Examiner respectfully submits that Applicants are free to define the invention in whatever fashion they choose. It is Applicants, not the Examiner, who must distinguish the claimed invention over the prior art, which includes inherently disclosed prior art and prior art which is old and well known.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. § 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. § 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. § 103(c) and potential 35 U.S.C. § 102(e), (f) or (g) prior art under 35 U.S.C. § 103(a).

9. Claims 1-2, 4-10, 12, 14-20, and 23 are rejected under 35 U.S.C. § 103(a) as being unpatentable over US Patent No. 5,371,878 to Coker in view of "How Debuggers Work" by Jonathan B. Rosenberg (Rosenberg).

Regarding claim 1, Coker teaches a method comprising:

In a microcontroller, executing a set of boot code to carry out initialization (“Embedded Computer System or ECS”, see column 1, lines 20-23) [*“[T]his invention uses hardware and software which can ‘shadow’ the execution of a target-ECS in real time operation”* (column 2, lines 34-40); *“A shadow system of this invention executes the same software as the target-ECS from system start-up or reset.”* (column 2, lines 56-58); Applicants’ remarks state that: “Bootting is a process that starts a system (e.g., operating system) and substantially initialize the system when a user turns on a computing system or a system with a processor.” (Applicants’ remarks, 6 February 2007, page 15)];

In a virtual microcontroller (“shadow system”), executing a set of timing code to enable the lock-step synchronization, wherein the timing code is timed to take the same number of clock cycles as the microcontroller uses to execute the boot code, [*“A shadow system of this invention executes the same software as the target-ECS from system start-up or reset.”* (column 2, lines 56-58); *“The shadow system and the target-ECS function exactly the same except that the shadow system receives data slightly delayed because of a data buffer between the target-ECS and the shadow system.”* (column 3, lines 13-16); *“[I]n terms of relative time, the execution state of the shadow system 28 at the time when any given instruction is executed will directly correspond to the execution state of the target-ECS when the same instruction was executed..”* (column 8, lines 44-49)]

and wherein at least one portion of said set of timing code is different from said set of boot code, [*“Thus, rather than receiving input data from an external source and reading the data into complex I/O registers, the shadow system uses the data value and relative time of input*

Art Unit: 2123

events from the target-ECS and writes the value directly to its RAM using its internally generated location.” (column 2, line 63 – column 3, line 1)];

and wherein the boot code is stored within the microcontroller and at least one portion of the boot code is inaccessible to the virtual microcontroller [Interface means 19 connecting the target-ECS and shadow system is used by Coker to transmit I/O data and does not appear to contain any suggestion that instruction code or boot code is transmitted via interface means. See (column 4, lines 9-18)].

Although Coker teaches “a computer system and method for debugging, verifying and developing an embedded computer system” (column 1, lines 9-11), Coker does not expressly teach old and well-known tools and techniques of debugging. As a result, Coker teaches a method of debugging, but does not expressly teach simultaneously halting both the microcontroller and the virtual microcontroller.

Rosenberg expressly teaches halting multiple processors operating in lockstep [*“A significant issue for debuggers on multiprocessor systems is how or whether other processors stop when a fault occurs in one. On SIMD architectures, by definition, all processors operate in lock step and so this is guaranteed.”* (page 45, first full paragraph)].

Rosenberg and Coker are analogous art because both are drawn to debugging.

It would have been obvious to a person of ordinary skill in the art at the time of Applicants’ invention to combine the teachings of Rosenberg and Coker because Rosenberg provides teachings specifically directed to debugging tools, which are suggested by Coker, but “are very difficult tools to build robustly because they depend heavily on relatively weak portions of operating systems and because they tend to stress the underlying operating system’s

Art Unit: 2123

capabilities.” (Rosenberg, page 1, first paragraph). That is, Rosenberg provides the teachings that provide helpful guidance in making and using the “critical tools for the development of software” (Rosenberg, page 1, first paragraph) that are suggested by Coker (title, abstract). The combination could be achieved as expressly taught by Rosenberg, by halting the target-ECS and the shadow system “simultaneously” because Rosenberg explicitly teaches this behavior in architectures, like the one claimed, that operate in lock step. (*Id.*)

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of Applicants’ invention to combine the teachings of Rosenberg and Coker to arrive at the invention specified in claim 1.

Regarding claim 2, Coker teaches copying register contents from the microcontroller to corresponding registers in the virtual microcontroller [“*An execution state, including the contents of RAM and I/O registers in the target-ECS and RAM and I/O state memory in the shadow system, can further be defined as including an input state vector, output state vector, and internal state vector. Input and output state vectors are defined as the contents of input and output registers respectively in the target-ECS and as the contents of the I/O memory state in the shadow system.*” (column 8, lines 50-57); copied from the target-ECS to the shadow system, “*the shadow system receives its input data from the input registers of the target-ECS and stores the input data in its RAM.*” (column 2, lines 61-63)].

Also, Rosenberg teaches that “*debuggers provide disassembly views and direct access to hardware registers.*” (page 6, first full paragraph).

Regarding claim 4, Rosenberg teaches that after executing code, a processor branches to an instruction line [*“A breakpoint is a special code placed in the executing code stream that, when executed, causes a special trap to occur that the processor and the operating system report to the debugger.”* (page 5, second full paragraph); More generally at pages 56-57, “Generic OS-Debugger Interaction Model”, etc.].

Regarding claim 5, Rosenberg teaches that prior to executing code, a break is set at an assembly instruction line [*“A breakpoint is a special code placed in the executing code stream that, when executed, causes a special trap to occur that the processor and the operating system report to the debugger.”* (page 5, second full paragraph)].

Regarding claim 6, Coker teaches that the boot code comprises protected initialization code that is not accessible to the In-Circuit Emulation system [Coker teaches no means by which the in-circuit emulation system may access the code on the target-ECS. Here Applicants’ have presented a negative limitation, which has been interpreted and treated according to MPEP 2173.05(i).].

Claim 7 recites a combination of limitations recited by claims 4 and 5, which are taught by Coker in view of Rosenberg as shown above.

Claim 8 recites a combination of limitations recited by claims 2, 4, and 5, which are taught by Coker in view of Rosenberg as shown above.

Regarding claim 9, Rosenberg teaches removing a break at an assembly line [*“Inactive breakpoints are place holders that the user can turn active but currently will not cause execution to stop if reached.”* (page 27)].

Claim 10 recites a combination of limitations recited by claims 1, 2, and 9. As Coker in view of Rosenberg teaches these claims, claim 10 is rejected for similar rationale.

Claims 12-20 present a broader recitation of claims 1-9. These claims are rejected for rationale similar to that given above for claims 1-9 as being obvious over Coker in view of Rosenberg.

Regarding claim 23, Coker teaches that at least on portion of the boot code is stored internally in said microcontroller [*“In other words, an ECS normally executes software...”* (column 1, lines 29-39); As noted above, Coker teaches no means by which the in-circuit emulation system may access the code on the target-ECS.].

10. Claim 21 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Coker in view of Rosenberg as applied to claim 12 above, and further in view of “Emulation of the Sparcle Microprocessor with the MIT Virtual Wires Emulation System” by Matthew Dahl, Jonathan Babb, Russel Tessier, Silvina Hanono, David Hoki, and Anant Agarwal (Dahl) and further in

Art Unit: 2123

view of “A Reconfigurable Logic Machine for Fast Event-Driven Simulation” by Jerry Bauer, Michael Bershteyn, Ian Kaplan, and Paul Vyedin (Bauer).

Coker in view of Rosenberg does not expressly teach that the shadow system is implemented on a field programmable gate array (FPGA).

Dahl teaches that it is known in the art to emulate a Sparc microprocessor using an FPGA (abstract).

Bauer teaches that hardware emulation can increase simulation speed by up to 10,000 times (introduction, paragraphs 1-2).

Therefore it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine these teachings and arrive at the decision to implement the shadow system of Coker on an FPGA to realize an enormous increase in simulation speed. Knowledge that this was possible is provided by Dahl, and motivation to combine the references, to increase simulation speed, is provided by Bauer.

Therefore it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the teachings of Coker in view of Rosenberg with Dahl and Bauer to arrive at the invention specified in claim 21.

11. Claim 22 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Coker in view of Rosenberg as applied to claim 1 above, and further in view of US Patent No. 4,757,534 to Matyas et al.

Regarding claim 22, Coker in view of Rosenberg does not disclose that the boot code comprises serial numbers, passwords, and algorithms.

Matyas teaches code that comprises serial numbers, passwords, and algorithms [*"In carrying out the computer/smart card protocol, the T output is sent to the smart card together with the parameters P1 (password) and P2 (program number | diskette serial number, where | denotes concatenation) and a third parameter P3. Where the crypto facility uses the DES algorithm, as shown in FIGS. 8 and 9, to encrypt the file key, P3 is the computer number."* (column 13, lines 1-21)].

Matyas and Coker in view of Rosenberg are analogous art because both are directed to computer software.

It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the teachings of Matyas with Coker in view of Rosenberg to include the passwords, serial numbers, and algorithms in the boot code in order to discourage "the copying and sharing of purchased software program" (here, the boot code) as expressly taught by Matyas (abstract). The combination could be achieved by implementing the smart card cryptographic method taught by Matyas with the target-ECS system taught by Coker.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the teachings of Matyas with Coker in view of Rosenberg to arrive at the invention specified in claim 22.

Conclusion

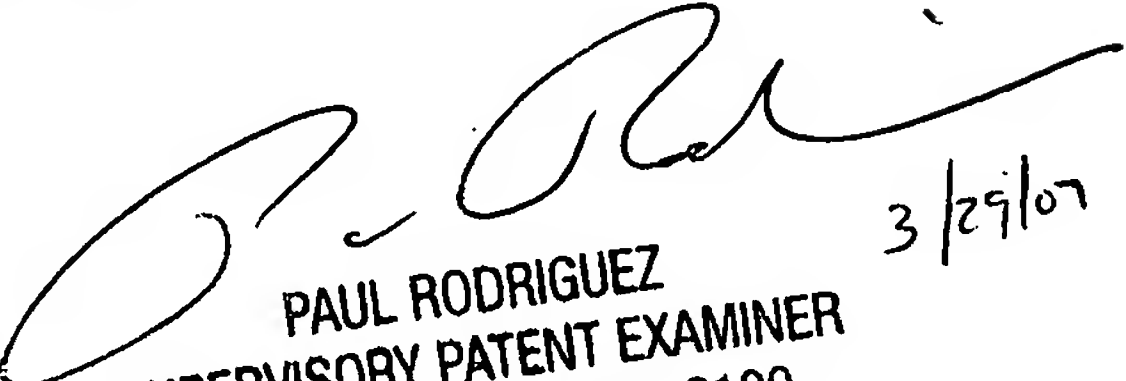
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached at (571) 272-3753. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason Proctor
Examiner
Art Unit 2123

jsp


PAUL RODRIGUEZ
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
3/29/07